ISSN:0975-9646

Deepak Mishra et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 3 (4) , 2012,4670 - 4673

Software Simulation of Unequal Error Protection Based Demodulator (Burst Mode) for Onboard Application

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***Abstract*—This paper describes the algorithm and implementation details of a new DSP based 64 Kbps Demodulator developed for onboard application. This demodulator has the capability of unequal error protection (UEP) based on multiple block coded modulation (MBCM). The software is run on ADSP-21020 simulator and MATLAB. The demodulator is tested by comparing the results of DSP simulation with original modulating Burst sequence baseband data. The test results are presented in the paper.**

Keywords- Prototype modem; UEP; MBCM;BER,Eb/No.

I.INTRODUCTION

In this paper, we describe a prototype demodulator which has the capability of unequal error protection (UEP) based on multiple block coded modulation (MBCM) [1]. In many applications, the transmitted data bits can be classified as the more important bits (MIB) and the less important bits (LIB) in terms of their sensitivity to channel errors. The basic task of UEP is to provide a smaller bit error rate (BER) for MIB than that for LIB [2, 3]. One advantage of using MBCM is that UEP can be achieved without compromising the performance of LIB and using only one channel encoder/decoder.

The new generation of satellite communication systems with regenerative transponders promise substantial benefits in overall system engineering. In this scheme, the uplink signal is demodulated onboard to recover the baseband data. Then a carrier is remodulated with the data, upconverted, amplified and transmitted as downlink.

This requires the use of an on-board QPSK demodulator. For this purpose, a 64 Kbps QPSK demodulator for Burst mode[4,5,6,7,8] has been developed at Space Applications Centre, ISRO, Ahmedabad, using digital signal processing techniques.

The major applications of UEP in our applications is detection of unique word(UW), which will be used to recognized the start of the burst data.

II.SPECIFICATIONS

The Table-1 gives overall specifications of the demodulator. The Table-2 gives the specifications used for the hardware platform. The Table-3 gives the specifications used for the implementation of algorithm based on digital signal processing techniques.

Table – 1 Overall Specifications of demodulator

Transmission data rate	64 Kbps
Input IF signal frequency	455 KHz
Modulation	QPSK
Mode	Burst
Phase ambiguity resolution	By differential encoding and decoding
Decision	Hard decision
Output signal	I and Q channel data
UEP Capabilty	Using MBCM Principle

Table – 2 Hardware Specifications

Processor	Analog Device chip ADSP-21020 (Radiation hardened version)
Clock Speed	18.432 MHz
ADC	8-bit
Pre-filter	Analog, 96 KHz bandwidth
Output	TTL, buffered

Table – 3Software Specifications

Processing mode	Block-by-block
Block length	18 bits
Mixer LO frequency	384 KHz with offset correction
Mixer output frequency	71 KHz
Samples/bit at input	12
ADC Sampling rate	1.536 Mbps
Samples/bit at IFIR heterodyne output	3

III. MBCM PRINCIPLE AND STRUCTURE OF DEMODULATOR

First, we briefly review the principle of MBCM using the generalized encoded bit matrix shown in Fig. 1. There are a total of k+2 bit levels in the matrix labeled as $l_1, l_2, \ldots, l_{k+2}$; a_i (i=1, 2, …, (n-1)k+n) denote date bits, and c_l (l=1, 2, …,k+1) parity check bits. It can be seen that a repetition code is applied at level l_1, while a single parity check code is applied repeatedly at the other levels.

One column of the encoded bit matrix corresponds to a branch of the code trellis. From each column, k symbols of

an 4-PSK are derived. We denote this as MBCM-k. The k symbols first take a bit from l_1 and another one from l_2.These two bits are used commonly in the k symbols as the first and second bits. Then, the k symbols take bits from l_3 through l_{k+2} , respectively, as their third bits. The two bit levels of an 4-PSK with the intraset distances of $d_1^2(l_1)$= 2.0 , and $d^2_{other}(l_{k=2})$= 4.0

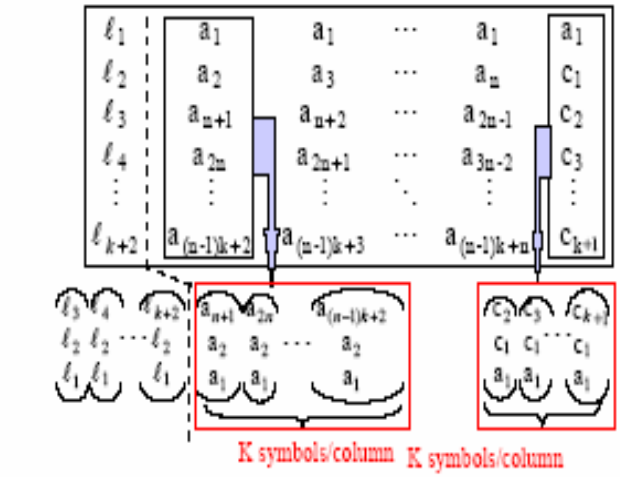

Fig.1. Encoded bit matrix and generation of channel symbol

For the minimum Hamming distance (MHD), using common bits for k symbols, the repetition code, and the parity check code provide the MHD of k, n, and 2, respectively. Thus, we have $\delta_1(l_1)$=k*2, and $\delta_2(l_{other})$=2. Consequently, the MSED for each level is given by

$$d_E^2(l_1)= d_1^2(l_1) \times \delta_1(l_1)= 4K$$

$$d_E^2(l_2)= d_E^2(l_{K+2})= d_2^2(l_2) \times \delta_2(l_2)=8.0 \quad \ldots\ldots\ldots\ldots(1)$$

This enables us to simultaneously increase the MSED at l_1 by increasing k, while the MSED at l_{other} keeps the value 8.0. The MSED at l_1 will be larger than that at l_{other} if k is equal to or larger than three and the code length n is equal to or larger than seven. One tradeoff in increasing k is decrease of transmission rate R_T (average data bits per channel symbol), which is given by

$$R_T = ((n-1)/n) + (1/k) \text{ (bits/symbol)} \quad \ldots\ldots(2)$$

The structure of the demodulator is described in figure – 2. The input QPSK modulated signal at 455 KHz is passed through an analog filter of 96 KHz bandwidth. The bandwidth of the filter allows us to upgrade the system for transmission rate of 128 Kbps. Then the signal is amplified for ±1 V peak-to-peak level before giving to S/H for sampling. The S/H circuit is clocked by a DDS NCO, which is controlled by DSP to sample at the required sampling rate. The S/H output is quanitized by an ADC for 8-bit resolution.

The samples are digitally processed by ADSP-21020. The samples are collected for 18 bits and stored in switching dual-buffer on continuous basis. The DSP processes the samples of a buffer and demodulates the data before the other buffer is filled fully.

The input samples of a block are first mixed with LO. The output of mixer is passed through Interpolated FIR filter and decimated to recover baseband. The output of IFIR is subjected to matched filtering for clock recovery and decision.

The raw I and Q channel data is integrated for phase error estimation over block. This is used to correct the LO frequency for carrier tracking.

The demodulator also implements carrier recovery to estimate the carrier frequency with sufficient accuracy at starting for locking.

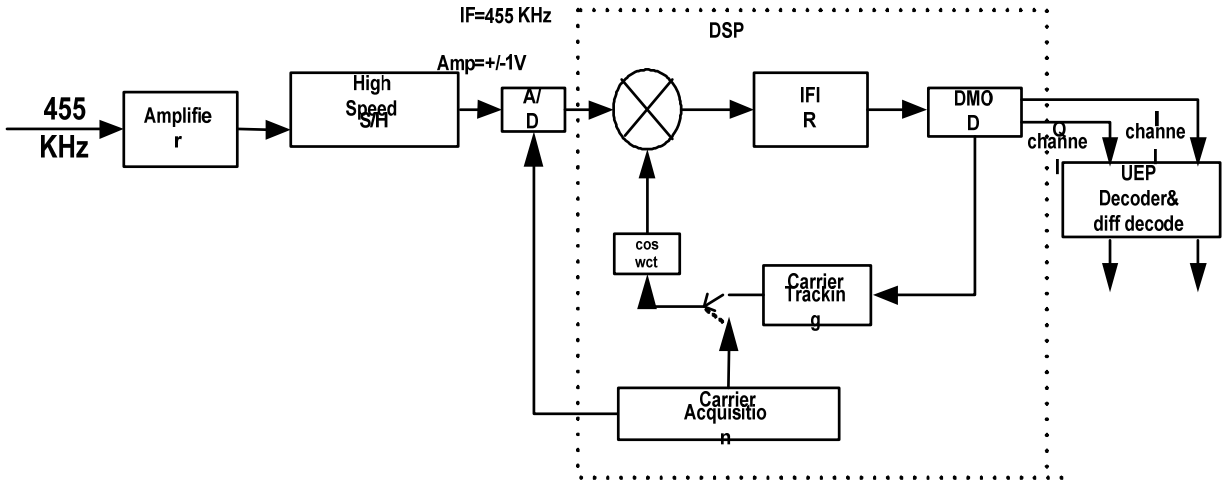

Fig. 2 Overall Block Diagram of Demodulator

IV. SOFTWARE STRUCTURE

The software flow of the demodulator using digital signal processing techniques is described in Fig-3.

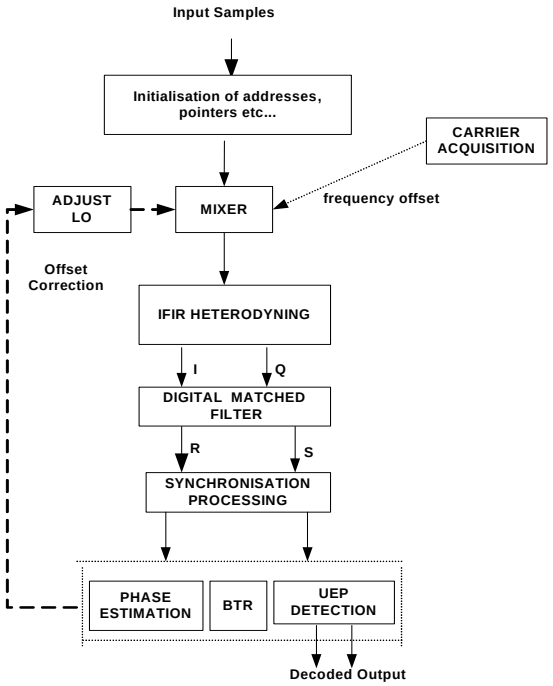

Fig. 3. SOFTWARE BLOCK SCHEMATIC OF DEMOD

As shown in the above figure, the samples of the input signal are acquired in two buffers and passed through the mixer to obtain the signal at lower IF for further processing. The samples at the output of the mixer are passed through the IFIR (Interpolated FIR) heterodyning stage to obtain the baseband I and Q data streams.

Digital matched filtering is done on these baseband signals. Its purpose is to increase the signal component and reduce the noise component at the same time thus maximizing the signal to noise ratio at the output at some instant. This is followed by synchronisation processing which involves baud synchronisation, phase estimation, coherent detection and differential decoding. Block phase estimator helps in frequency tracking and the frequency offset correction is applied for the next block of data through NCO. The demodulator here requires an initial carrier reference during start and this is obtained from the carrier acquisition module. It makes the required correction to the local oscillator of the mixer.

V.MAJOR MODULES

The sampling frequency is 1.536 Mbps and the main program sets NCO for this frequency. There are 24 samples per bit and actual demodulation is done on block by block basis where each block is of 18 bits.

5.1 Acquiring Data Samples
5.2 Mixers
5.3 IFIR Heterodyning
5.4 Digital Matched Filtering
5.5 Synchronization processing
5.6 Phase Estimation
5.7 Coherent Detection
5.8 Differential Decoder

VI. TEST METHODOLOGY

The software is run on ADSP-21020 simulator. To feed data of the required input signal to the demodulator, a QPSK modulator program written in MATLAB is used. The UEP scheme applied on unique word and rest of data . The QPSK modulator program uses UEP data sequence as baseband data and adds AWGN noise to the modulated signal. Thus, it can generate the signal of different Eb/No. The output of the QPSK modulator goes to a file, which is read into the input buffers of the DSP program.

The output of the DSP program is stored in a file. This file is compared with the original baseband data file in MatLab and BER is found.

VII. TEST RESULTS

The results are presented below for 1 block of data. Figure 4 shows the BER performance with and without UEP.It has been seen that BER performance of UEP based demodulator is better in comparison from without UEP based demodulator. Figure 5 reflects the improvement in BER with respect to increase in overhead at different Eb/No.

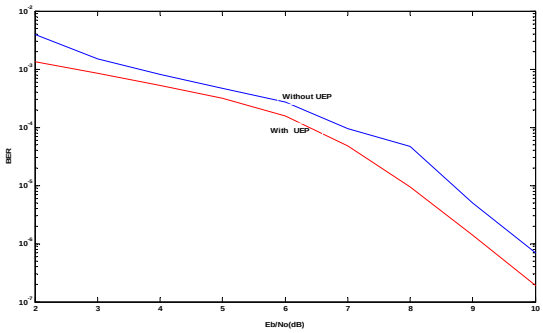

Fig. 4. BER curve at different Eb/No

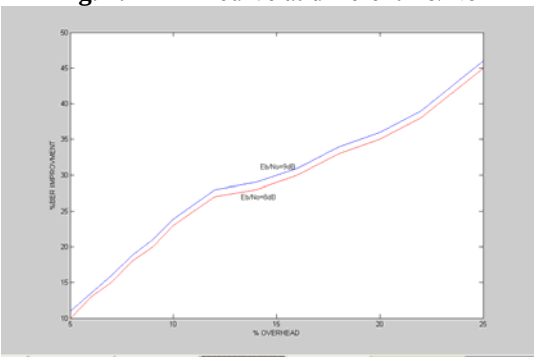

Fig. 5. %BER improvement at different overhead

Figure 6 shows the phase plot of the demodulator. The phase is obtained at the end of each block.

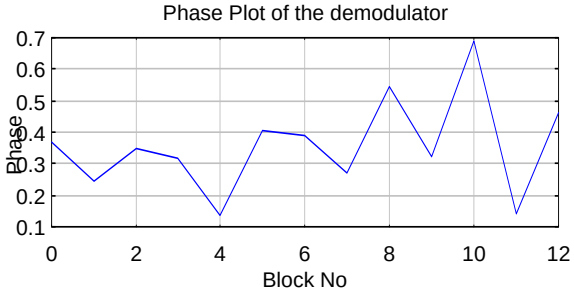

Fig. 6 . Phase Curve

VIII. CONCLUSION

The 64 Kbps demodulator with UEP capabilities implemented on ADSP-21020 platform using digital signal processing techniques meets the performance standards.
It has been seen that BER performance of DSP based demodulator is improved using UEP algorithim. It can be used for faster access in various satellite applications.

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